MPFC-440-3PH-400-LE
Power Factor Correction Large-Module

Military Grade 3-Phase Power Factor Correction Module

440 Vrms L-L Δ	47 Hz to 800 Hz	400 Vdc	5.0 kW	@ 80 °C	200 kHz	97%
Input Voltage	Input Frequency	Output Voltage	Output Power	Baseplate Temp	Sw Freq	Full Load Efficiency

The MilCOTS 3-Phase MPFCQor Power Factor Correction module is an essential building block of an AC-DC power supply. Used in conjunction with one of SynQor's matched 3-Phase AC line filters and a limited amount of stabilizing capacitance, this MPFCQor will draw well-balanced and low-distortion sinusoidal currents from each phase of a 3-Phase AC input. It is designed to comply with a wide range of military standards and is manufactured in the United States.

MPFCQor™

Designed and manufactured in the USA

Operational Features

- Large-module form factor
- 5.0 kW continuous rating at 80 °C baseplate temperature
- Semi-regulated output: 400 Vdc
- Compatible with Military Standard 60 Hz, 400 Hz & var. freq. systems
- Meets military standards for harmonic content
- Drives pulsed output loads without passing transients back to the input (requires adequate capacitance; see pulsed loads section)
- Minimal inrush current
- Balanced phase currents
- High power factor (0.999 at 60 Hz / 5.0 kW)
- Minimal external output capacitance needed
- Supports full load current during startup ramp
- Additional input filters available to meet full EMI
- N * 5.0 kW power levels when paralleled

Control Features

- All control pins referenced to separate floating return
- Asynchronous serial data interface
- AC and DC Power Good outputs
- PFC Enable and Battle Short inputs
- 3.3 V always-on standby power output
- Clock synchronization output

Protection Features

- Output current limit and auto-recovery short circuit protection
- Auto-recovery input under/over-voltage protection
- Auto-recovery output over-voltage protection
- Auto-recovery thermal shutdown

Compliance Features

3-Phase PFCQor series converters are designed to meet:
(With an MCOTS 3-Phase AC input filter)

- MIL-STD-461 (C, D, E, F)
- MIL-STD-1399 (at 440 Vrms L-L)
- MIL-STD-810G

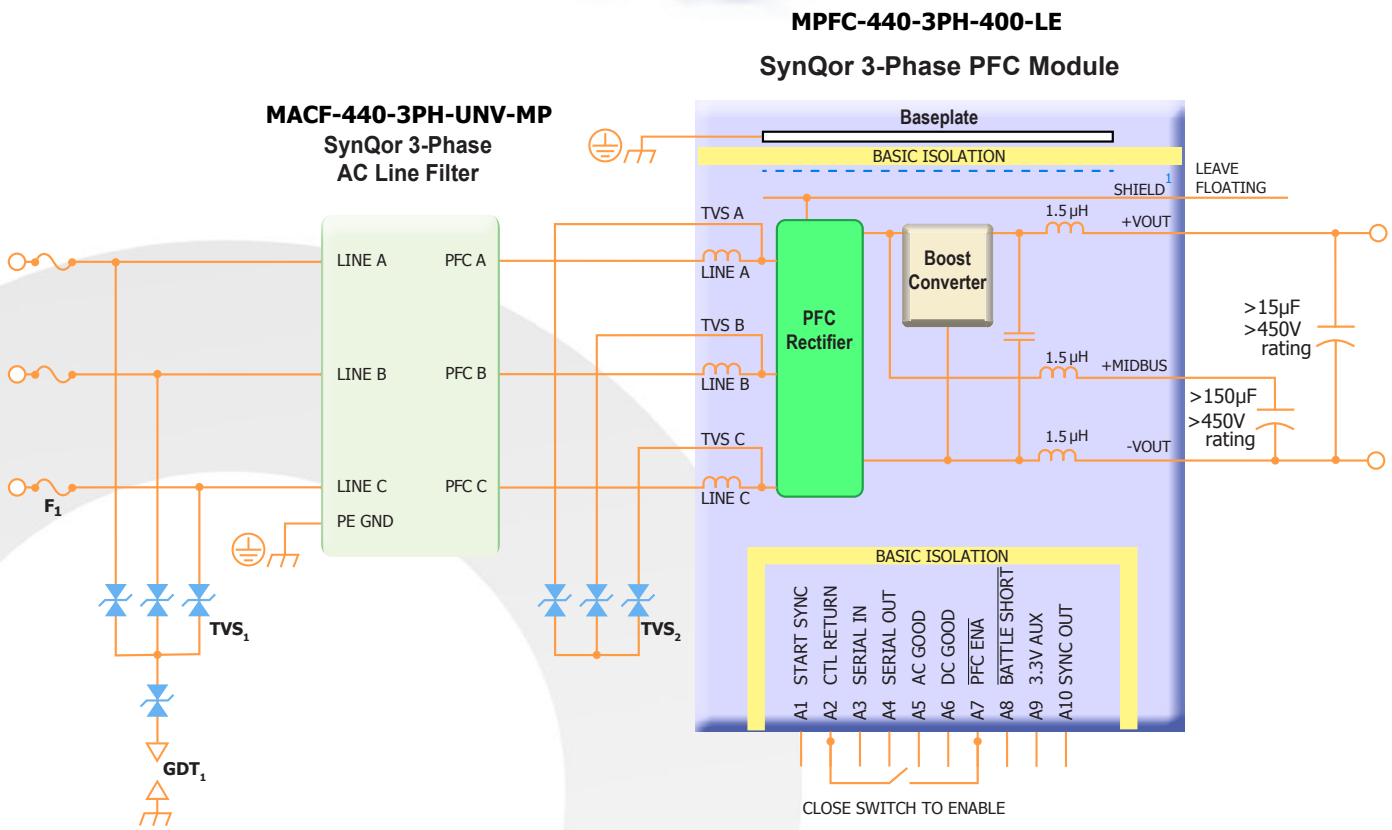
Mechanical Features

- Size: 7.320" x 4.920" x 0.602" (186 x 125 x 15.3 mm)
- Weight: 36 oz (1020 g)

Contents Features

MPFC-440-3PH-400-LE

Input: 3Φ 360-528 Vrms (L-L)
Output: 400 Vdc
Power: 5.0 kW



1 SHIELD pin must be left floating, but may be externally connected to plane under unit near top of PCB to contain high frequency EMI.

Suggested Parts:

TVS $_1$:	430 Vpk, 10 kA; Littelfuse AK10-430C or Bourns PTVS10-430C-TH
TVS $_2$:	430 Vpk, 3 kA; Littelfuse AK3-430C or Bourns PTVS3-430C-TH
GDT $_1$:	1.5 kV, 3 kA; Littelfuse GTCA28-152M-R03
F $_1$:	500 VAC, 30 kA; Littelfuse 0505020.MXEP

Figure A: Typical application with matched input filter and MPFCQor module

MPFC-440-3PH-400-LE Electrical Characteristics

Operating Conditions: 440 Vrms L-L (254 Vrms L-N) 3-Phase 60 Hz; 5.0 kW output; baseplate temperature = 25 °C unless otherwise noted. Full operating baseplate temperature range is -55 °C to +100 °C (derated above 80 °C). Specifications subject to change without notice.

Parameter	Min.	Typ.	Max.	Units	Notes & Conditions
ABSOLUTE MAXIMUM RATINGS					
Input Voltage at TVS Pins			1150	Vpk L-L	Difference between pins TVS A/B/C
SERIAL IN and PFC ENA inputs	-2		7	V	Relative to CTL RETURN pin
AC GOOD, DC GOOD, and BATTLE SHORT outputs					
Pull Up Voltage	-2		7	V	Relative to CTL RETURN pin
Sink Current			10	mA	
Operating Temperature	-55		100	°C	Baseplate temperature (derated above 80 °C)
Storage Temperature	-65		135	°C	
INPUT CHARACTERISTICS					
Operating Input Voltage Range	360	440	528	Vrms L-L	3-Phase Δ (neutral not used); 208 to 305 Vrms L-N
Input Overvoltage Protection (between any two line inputs)		900		Vpk L-L	
Operating Input Frequency	47		800	Hz	
Source Inductance			300	uH	Per phase
Recommended Operating Range with Line Imbalance					
Amplitude Imbalance			20	Vrms L-L	
Phase Imbalance			5	deg	
Thresholds for Phase Imbalance Warning/Shutdown					See "Phase Imbalance Shutdown" section
Amplitude Imbalance		70		Vrms L-N	
Phase Imbalance		17		deg	
Inrush Current (output disabled; input ramped over 16.7 ms)			0.5	A	All output cap remains discharged due to buck PFC
Power Factor		0.999			60 Hz, 5.0 kW
Total Harmonic Distortion of AC Input Current		0.6	2	%	Full load (see figure for data vs. load)
Reactive Power (per phase)					Disabled (see note 1); Leading
400Hz		120		VAR	Active cancellation in effect running > 1 kW (see fig)
60Hz		18		VAR	Active cancellation in effect running > 500 W
Enabled AC Input Power, No Load (sum of phases)					See note 1
400Hz		13		W	
60Hz		9.4		W	
Disabled AC Input Power (sum of phases)					See note 1
400Hz		11		W	
60Hz		7.0		W	
Maximum Input Current (per phase)			9	Arms	360 Vrms L-L, 5.0 kW
+VOUT OUTPUT CHARACTERISTICS					
+VOUT Steady-State Voltage at 1 A Load		404		V	
+VOUT Output Voltage at 12.8 A Load		392		V	See figure "+VOUT voltage vs. load current"
+VOUT Steady-State Voltage Ripple					With nominal +VOUT capacitance and balanced line
Peak-to-Peak (DC to 10 MHz)		1.0		Vpk-pk	
RMS Ripple (DC to 10 MHz)		0.1		Vrms	
Recommended +VOUT Capacitance	15	15	400	uF	Use R || D for additional cap
Output Over-Voltage Limit Threshold (full temp range)	440	454	470	V	Cycle-by-cycle limit, guaranteed by design
+MIDBUS CHARACTERISTICS					
+MIDBUS Current Limit Setpoint	21.0	22.5	24.0	A	See graph of available power vs. input line voltage
Recommended +MIDBUS Capacitance	150	200	1000	uF	Use R || D for additional holdup cap
EFFICIENCY					
From AC 3-Phase Input to Main Output					
100% Load (5.0 kW)		97.4		%	
25% Load (1.25 kW)		97.1		%	
DYNAMIC CHARACTERISTICS					
Turn-On Transient					
Start-up Inhibit Time		300		ms	From PFC ENA to 10% nominal +VOUT
Turn-On Time		550		ms	From PFC ENA to 100% nominal +VOUT
Auto-Restart Time		1		s	See "Protection Features" in application section

Note 1: External input filter will contribute to this parameter; refer to the appropriate filter datasheet.

MPFC-440-3PH-400-LE Electrical Characteristics (continued)

Operating Conditions: 440 Vrms L-L (254 Vrms L-N) 3-Phase 60 Hz; 5.0 kW output; baseplate temperature = 25 °C unless otherwise noted. Full operating baseplate temperature range is -55 °C to +100 °C (derated above 80 °C). Specifications subject to change without notice.

Parameter	Min.	Typ.	Max.	Units	Notes & Conditions
FEATURE CHARACTERISTICS					
SERIAL IN					
Idle / Stop State Input Voltage	2.4			V	
Zero / Start State Input Voltage			0.8	V	
Internal Pull-Up Voltage		3.3		V	
Internal Pull-Up Resistance		10		kΩ	
SERIAL OUT					
Idle / Stop State Output Voltage	2.9	3.1		V	4 mA source current
Zero / Start State Output Voltage		0.2	0.4	V	4 mA sink current
AC GOOD (positive logic)					Startup inhibited until AC GOOD output high
Input Voltage Low Threshold		343		Vrms L-L	AC GOOD low below this threshold
Input Voltage High Threshold		558		Vrms L-L	AC GOOD low above this threshold
Hysteresis of Input Voltage Thresholds		3.5		Vrms L-L	Raises low threshold and lowers high threshold
Line Frequency Low Treshold	43	45	47	Hz	AC GOOD low below this threshold
Line Frequency High Threshold	860	900	940	Hz	AC GOOD low above this threshold
Hysteresis of Line Frequency Tresholds		0		Hz	
Low State Output Voltage		0.2	0.4	V	2 mA sink current
Internal Pull-Up Voltage		3.3		V	
Internal Pull-Up Resistance		10		kΩ	
DC GOOD (positive logic)					DC Power Good output
Rising threshold		360		V	DC GOOD high above this threshold
Falling threshold		210		V	DC GOOD low below this threshold
Low State Output Voltage		0.2	0.4	V	2 mA sink current
Internal Pull-Up Voltage		3.3		V	
Internal Pull-Up Resistance		10		kΩ	
$\overline{\text{PFC ENA}}$ (negative logic)					PFC enable input (pull low to enable unit)
Off State Input Voltage	2.4			V	
On State Input Voltage			0.8	V	
Internal Pull-Up Voltage		3.3		V	
Internal Pull-Up Resistance		10		kΩ	
$\overline{\text{BATTLE SHORT}}$ (negative logic)					Battle short input (pull low to disable protection)
Normal State Input Voltage	2.4			V	
Protection-Disabled State Input Voltage			0.8	V	
Internal Pull-Up Voltage		3.3		V	
Internal Pull-Up Resistance		10		kΩ	
3.3V AUX					3.3 V output always on regardless of $\overline{\text{PFC ENA}}$ state
Output Voltage Range	3.19	3.30	3.43	V	Over line, load, temp, and life
Source Current			100	mA	
SYNC OUT					Synchronization output at switching frequency
High State Output Voltage	2.9	3.1		V	4 mA source current
Low State Output Voltage		0.2	0.4	V	4 mA sink current
Buck Switching Frequency	190	196.5	203	kHz	Over temp and life
Boost Switching Frequency	380	393	406	kHz	Over temp and life; boost synchronized to buck
ISOLATION CHARACTERISTICS					
Isolation Voltage (Any Pin to Baseplate)			3000	V	Basic insulation
Capacitance (Pin 1-10 to Baseplate)		8		nF	
Isolation Voltage (Pin 1-10 to CTL RETURN)			3000	V	Basic insulation
Capacitance (Pin 1-10 to CTL RETURN)		750		pF	
Isolation Resistance	100			MΩ	
TEMPERATURE LIMITS FOR POWER DERATING CURVES					
Semiconductor Junction Temperature			125	°C	
Board Temperature			125	°C	
Transformer Temperature			125	°C	
Maximum Baseplate Temperature, Tb			100	°C	Derated above 80 °C
Over-Temperature Protection					Measured at surface of internal PCB
Disable Threshold		120		°C	
Warning Threshold		115		°C	Warning causes $\overline{\text{BATTLE SHORT}}$ pin to go high
Enable Threshold		115		°C	
RELIABILITY CHARACTERISTICS					
Calculated MTBF (MIL-217) MIL-HDBK-217F		700		10^3 Hrs.	Ground Benign, Tb = 70 °C
Calculated MTBF (MIL-217) MIL-HDBK-217F		100		10^3 Hrs.	Ground Mobile, Tb = 70 °C
Field Demonstrated MTBF				10^3 Hrs.	See our website for details

Mil-COTS MIL-STD-810G Qualification Testing

MIL-STD-810G Test	Method	Description
Fungus	508.6	Table 508.6-I
Altitude	500.5 - Procedure I	Storage: 70,000 ft / 2 hr duration
	500.5 - Procedure II	Operating: 70,000 ft / 2 hr duration; Ambient Temperature
Rapid Decompression	500.5 - Procedure III	Storage: 8,000 ft to 40,000 ft
Acceleration	513.6 - Procedure II	Operating: 15 g
Salt Fog	509.5	Storage
High Temperature	501.5 - Procedure I	Storage: 135 °C / 3 hrs
	501.5 - Procedure II	Operating: 100 °C / 3 hrs
Low Temperature	502.5 - Procedure I	Storage: -65 °C / 4 hrs
	502.5 - Procedure II	Operating: -55 °C / 3 hrs
Temperature Shock	503.5 - Procedure I - C	Storage: -65 °C to 135 °C; 12 cycles
Rain	506.5 - Procedure I	Wind Blown Rain
Immersion	512.5 - Procedure I	Non-Operating
Humidity	507.5 - Procedure II	Aggravated cycle @ 95% RH (Figure 507.5-7 aggravated temp - humidity cycle, 15 cycles)
Random Vibration	514.6 - Procedure I	10 - 2000 Hz, PSD level of 1.5 g^2/Hz (54.6 g_{rms}), duration = 1 hr/axis
Shock	516.6 - Procedure I	20 g peak, 11 ms, Functional Shock (Operating no load) (saw tooth)
	516.6 - Procedure VI	Bench Handling Shock
Sinusoidal vibration	514.6 - Category 14	Rotary wing aircraft - helicopter, 4 hrs/axis, 20 g (sine sweep from 10 - 500 Hz)
Sand and Dust	510.5 - Procedure I	Blowing Dust
	510.5 - Procedure II	Blowing Sand

Mil-COTS Converter and Filter Screening

Screening	Process Description	S-Grade	M-Grade
Baseplate Operating Temperature		-55 °C to +100 °C	-55 °C to +100 °C
Storage Temperature		-65 °C to +135 °C	-65 °C to +135 °C
Pre-Cap Inspection	IPC-A-610, Class III	•	•
Temperature Cycling	MIL-STD-883F, Method 1010, Condition B, 10 Cycles		•
Burn-In	100 °C Baseplate	12 Hours	96 Hours
Final Electrical Test	100%	25 °C	-55 °C, +25 °C, +100 °C
Final Visual Inspection	MIL-STD-883F, Method 2009	•	•

Power Topology Overview

A block diagram of this PFC rectifier may be seen in Figure A on page 2. A nominal input of 440 Vrms (L-L) / 254 Vrms (L-N) 3-phase Δ is presented at the LINE A/B/C pins, and an active-PFC buck converter creates a loosely regulated DC output between the +MIDBUS and -VOUT pins. This is a true 3-phase rectifier topology, as opposed to a composite of three single-phase rectifiers. An additional cascaded boost stage sits between +MIDBUS (the PFC buck output) and +VOUT, which will activate during brownouts or input dropout events to maintain regulation at +VOUT. Holdup capacitance may be added either at +MIDBUS or +VOUT to ride through longer dropout events. Both outputs are referenced to the –VOUT pin and are *not* isolated from the line inputs (see Figure 10).

The term "line-to-neutral (L-N) voltage" is sometimes used in this document even though this converter does not utilize a neutral wire. If a neutral wire is present in the application, it should not be connected to the PFC.

Performance

Efficiency and Power Dissipation

Efficiency running from 60 Hz is shown in Figure 1, with corresponding power dissipation in Figure 2 and variance over temperature in Figure 5.

Efficiency running at 400 Hz is shown in Figure 3, with corresponding power dissipation in Figure 4.

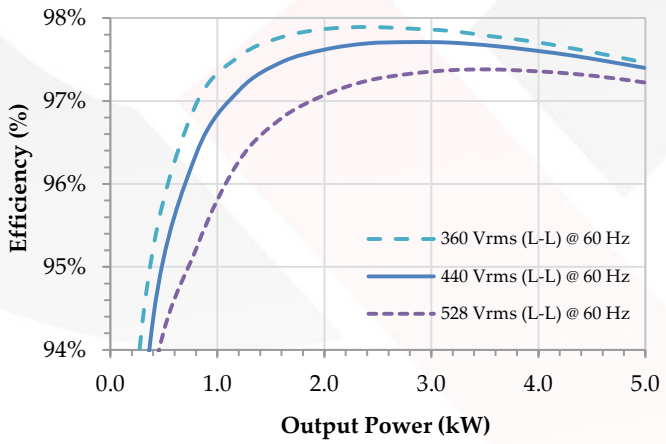


Figure 1: Efficiency vs. output power at 60 Hz input. Baseplate temperature: 25 °C.

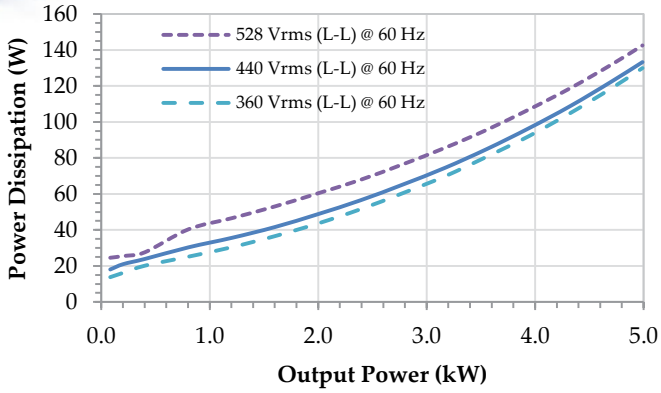


Figure 2: Power dissipation vs. output power at 60 Hz input (also see Figure 5). Baseplate temperature: 25 °C.

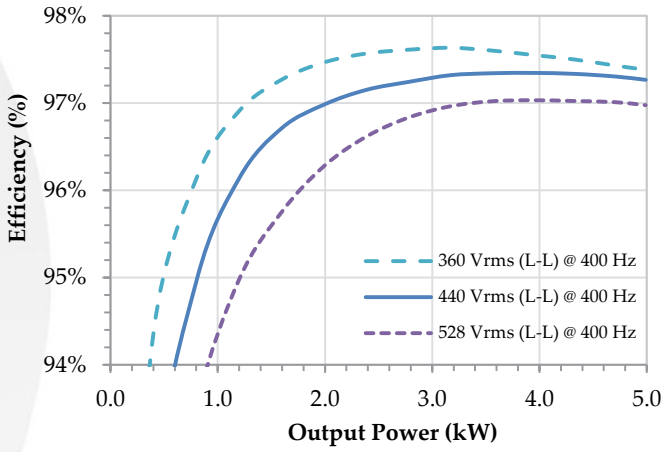


Figure 3: Efficiency vs. output power at 400 Hz input. Baseplate temperature: 25 °C.

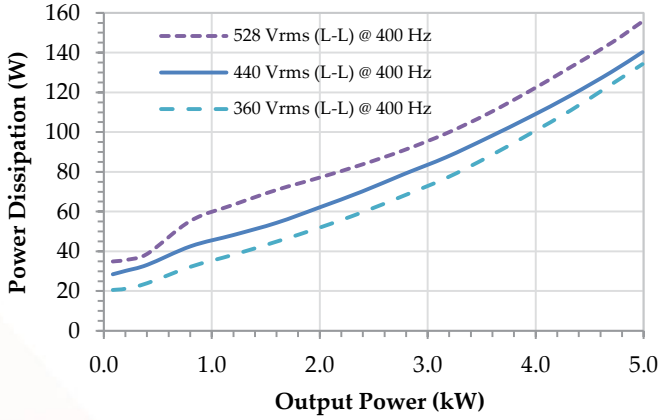


Figure 4: Power dissipation vs. output power at 400 Hz input. Baseplate temperature: 25 °C.

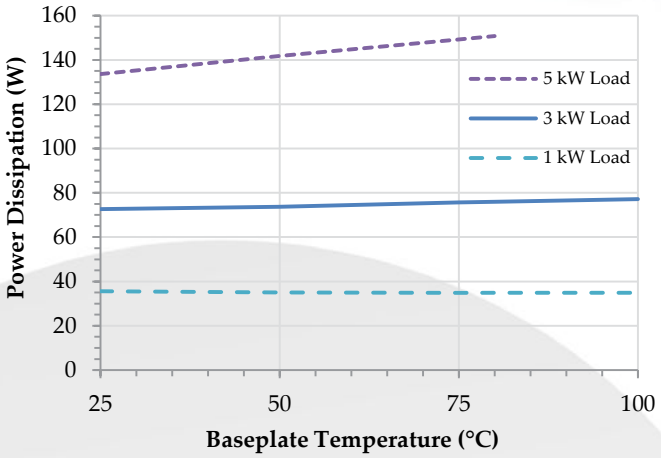


Figure 5: Power dissipation vs. baseplate temperature. Input at 3-phase 440 Vrms (L-L) and 60 Hz (also see Figure 2). Also see derating chart shown in Figure 14.

Input Current Distortion

Legacy diode rectifier solutions typically use bulky magnetics, while having relatively high distortion at line harmonics. In contrast, this modern true 3-phase PFC rectifier switches at high frequency, providing for very low distortion while using small and light internal magnetics. Active current control yields low harmonic content and well-balanced phase currents, even with phase and/or amplitude imbalance on the line inputs.

Input current harmonic content is typically excellent above 50% of full rated output power, increasing at light loads due to buck converter discontinuous mode operation (see Figure 6).

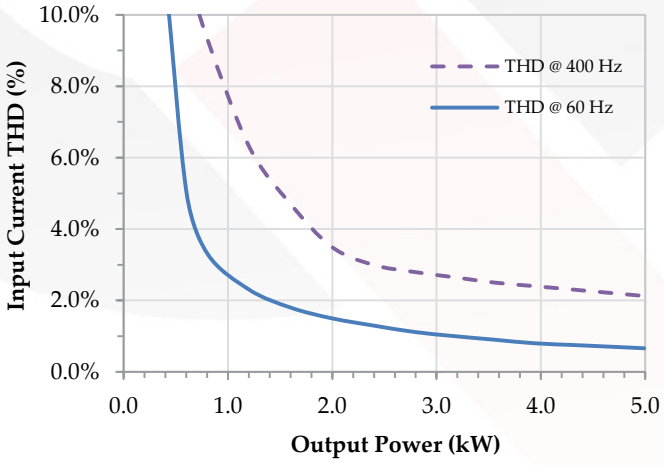


Figure 6: Input Current THD over full load range; input 3-phase 440 Vrms (L-L); includes external input filter module, part number MACF-440-3PH-UNV-MP.

Reactive Power at Fundamental

Line capacitance is necessarily integral to the input EMI filter circuitry, which is divided between internal filtering and the separately available external MACF-440-3PH-UNV-MP matched input filter module. Total reactive power (including this external input filter module) is approximately 240 VAR per phase when running at 400 Hz, and proportionately lower running at 60 Hz. When the output power is high enough, the PFC stage is actually able to cancel out this capacitive reactive power by drawing the proper level of inductive (lagging) input current. Figure 7 shows power factor as a function of output power. Above 1.0 kW at 400 Hz and above 0.5 kW at 60 Hz, this cancellation makes the overall power factor almost exactly unity (very slightly lagging).

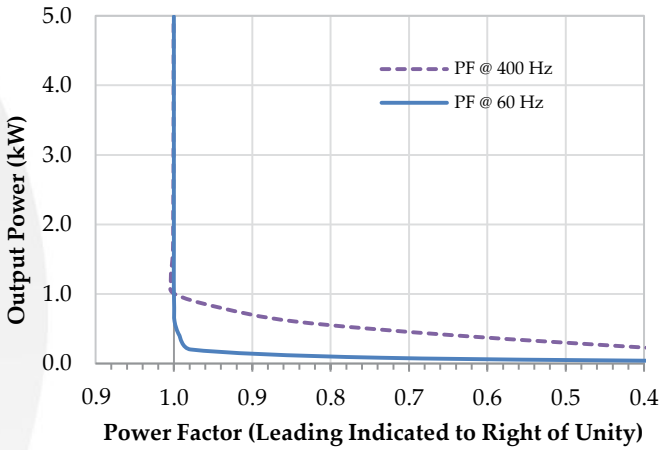


Figure 7: Input leading power factor as a function of operating power level at 3-phase 440 Vrms (L-L); includes MACF-440-3PH-UNV-MP external input filter module.

Operation near unity power factor can be seen directly in Figure 8, where input current and voltage have the same phase, crossing zero simultaneously. At low output power, the PFC stage is unable to do any compensation because its input currents are also low, and the phase of the input current reverts back to a capacitive leading 90 degrees.

The reactive power compensation scheme relies on advance knowledge of the total value of EMI capacitance present. *This expected capacitance value is programmable via the serial port at address 0x72 / 114 / "r".* The default power-up value is 1.5 µF, representing the sum of the input capacitance inside the PFC module (0.68 µF), the expected additional capacitance inside the external MACF-440-3PH-UNV-MP input filter module (0.68 µF), and an extra 0.14 µF to account for component tolerances and to bias the input current phase slightly lagging. These capacitance values are specified per-phase (L-N), assuming a lumped model with three such capacitors connected in a wye configuration from a floating center node to LINE A/B/C. If a different value of compensation

capacitance is desired, it needs to be specified at boot time on each power-up; this value is volatile and will revert to default after loss of power. It is acceptable to change this value on the fly while running. A value of zero will disable correction.

The angle of input current drawn by the power stage of the PFC (relative to the applied input voltage angle) may be read via the serial port at address 0x6B / 107 / "k".

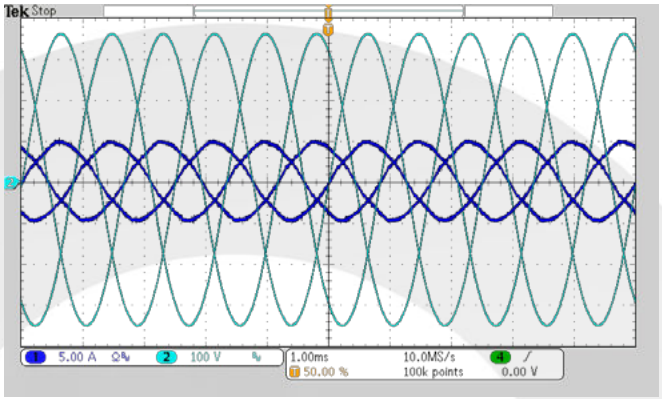


Figure 8: Typical 400 Hz input voltage and current waveforms at 2.5 kW output power (3 scope images superimposed); includes MACF-440-3PH-UNV-MP external input filter module.

Power Circuitry Overview

Inrush and Startup

Only a small amount of EMI capacitance resides before the main switches. The PFC buck topology avoids the large inrush events seen with traditional boost topologies, allowing large capacitors at the output to be charged with an actively controlled current limit. Figure 9 shows a typical startup initiated by $\overline{\text{PFC ENA}}$ (with line voltage already stable and AC GOOD high).

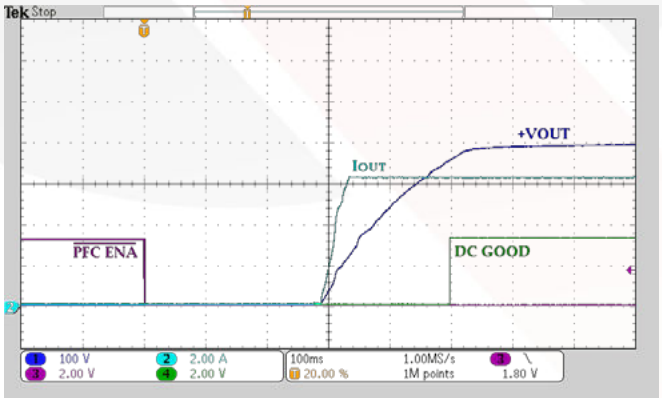


Figure 9: Startup into constant-current 6.3 A electronic load: +VOUT relative to –VOUT; otherwise relative to CTL RTN.

The unit will wait to startup until the AC GOOD signal is asserted and the $\overline{\text{PFC ENA}}$ input is pulled low. The AC GOOD signal will be asserted when all of the following three conditions are met:

1) the input frequency is within the valid AC GOOD range (see specification pages for levels and tolerance)
2) the input voltage is within the valid AC GOOD range (see specification pages for levels and tolerance)
3) the input phase voltages are adequately clean and balanced (specifically that ΔV_{sys} is less than threshold; see section entitled "Phase Imbalance Shutdown")

Line Transients

The input stage implemented in this module offers far better immunity from input surges than a traditional boost topology. In a traditional boost PFC, there is no mechanism to limit current flow directly from input to output during operation, so for long duration surges, the current becomes very large and results in permanent destruction of the power stage. In contrast, the buck PFC input stage used in this module is able to interrupt current flow during a voltage surge by simply turning off the series control switches, dramatically lowering device stresses.

External TVS devices are required at the input to keep the buck input voltage below the 1150 Vpk (L-L) absolute maximum rating. Dedicated pins are provided to connect these TVS devices directly across the internal power switches. This TVS network clamps any over-ringing during input transients caused by input filtering components inside the PFC module. See Figure A on page 2 for an example application circuit diagram including recommended TVS part numbers.

Line Frequency and Phase Rotation

Input frequency transients with high slew rates are handled seamlessly while running across the full 45 – 800 Hz range. The unit operates equally well with either ABC or CBA input voltage phase rotation. *The line input frequency may be read via the serial port at address 0x46 / 70 / "F". CBA rotation is indicated by a negative frequency.*

Common Mode Voltage

The +VOUT and +MIDBUS outputs share a –VOUT return, and all three pins are non-isolated with respect to the 3-phase line inputs. Measured relative to the line neutral wire (not used by the PFC module), the –VOUT pin inherently has common-mode ripple voltage at 3x line frequency and approximately 100 Vpk-pk (at nominal line voltage). This is shown in Figure 10, where each signal is measured using a differential probe referenced to the line neutral voltage. This large common-mode ripple is normally not observable, because differentially, the voltage from +VOUT to –VOUT is DC, with low ripple and noise as shown in Figure 11.

Nonetheless, it is important to understand that the output pins *are not isolated* from the input, so for safety purposes the outputs should be treated similarly to the AC line inputs.

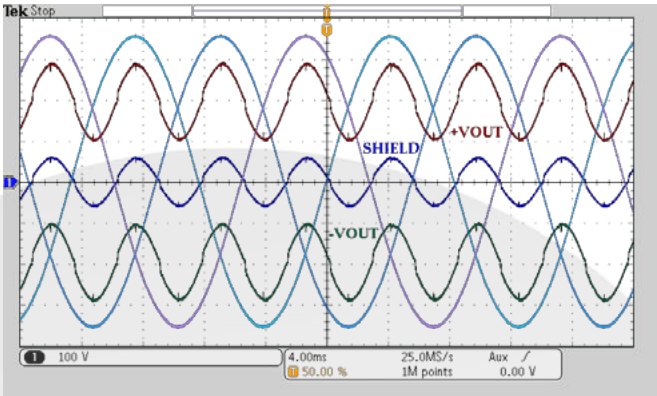


Figure 10: Typical input *and non-isolated output* pin voltages relative to the AC line neutral voltage (neutral connection not used by PFC); 60 Hz, 2.5 kW load.

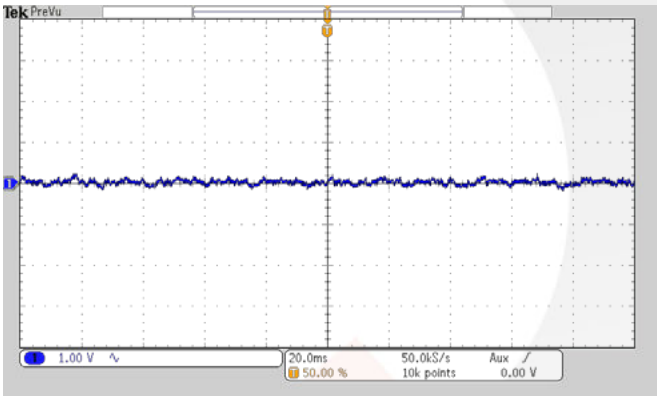


Figure 11: Differential output voltage ripple between +VOUT and –VOUT; 60 Hz input, 2.5 kW load.

Regulation vs. Line Voltage

Being a buck converter, the main PFC rectifier can only create a +MIDBUS output lower than the instantaneous line-to-line input voltage. Therefore, when the AC input is below 344 Vrms (L-L), the loosely-regulated 400 V steady-state +MIDBUS setpoint is reduced (see Figure 13).

The cascaded boost stage compensates for variations at +MIDBUS. The boost stage is limited to 50% duty cycle, so accounting for losses and assuming the unit is operating within its power rating (see Figure 13), +VOUT will remain regulated when the +MIDBUS voltage is greater than 215 V. For input voltages in the normal specified operating range 360 – 538 Vrms (L-L), the boost stage is turned off, and +MIDBUS is shorted to +VOUT by a bypass switch. This improves efficiency during steady-state operation, keeping the boost converter in reserve to handle line brownout / dropout events.

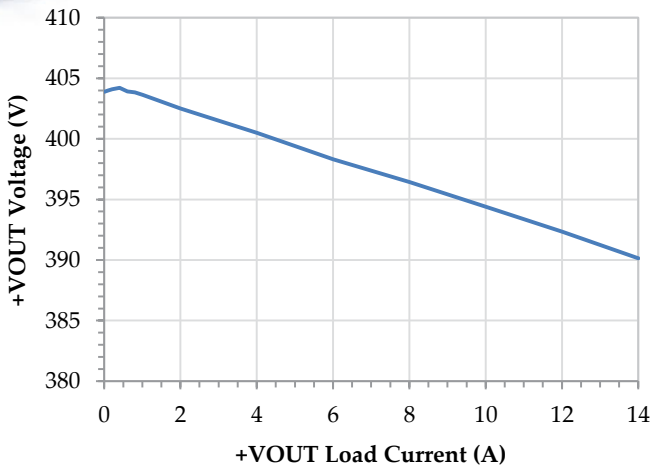


Figure 12: +VOUT voltage vs. load current: a controlled droop characteristic.

Paralleling Guidelines

Several control features to facilitate paralleling are available in the standard model. Up to 10 units may be paralleled with outputs directly connected. (More than 10 units may be paralleled when bus converters are used to isolate each PFC output.) Current sharing is achieved via the output voltage droop characteristic shown in Figure 12 above. This sharing method is inherently simple and robust: it is distributed (no master/slave), and involves no communication between units.

Reverse Power Flow

The buck PFC rectifier inherently can only deliver power in the forward direction because each input switch is wired in series with a high voltage diode. The same is true of the boost stage which uses a high voltage diode rectifier. Therefore, current cannot flow backwards from one unit into the output of another unit.

Control Features for Paralleling

Several special features are included to facilitate paralleling:

1) The START SYNC pin at location A1 should be wired together between all paralleled units. This actively aligns the restart time between units following an event that causes units to enter hiccup-mode. For instance, when full load is applied, one or more units could experience over-temperature shutdown, causing the remaining units to engage current limit, and 50 ms later entering hiccup due to +MIDBUS under-voltage shutdown. When these units attempt to restart, they may not start because some units are still forced off due to high temperature and the remaining units cannot support full load. When all the units are cool enough to

restart, the hiccup times between all units will probably not be aligned, so without START SYNC, the system may still not start. The START SYNC feature delays restart until all units are out of the hiccup state, so that all units will start up simultaneously.

2) The "E" serial port command automatically assigns a unique "Net Address" to each unit in the system. All units must be disabled at the time this command is issued. Each unit has a unique 120-bit number stored in ROM, which is encoded onto the START SYNC bus during this enumeration process. The resulting assigned "Net Address" may be used with a shared serial port to communicate individually to each unit in a paralleled system. The "Net Address" reverts to the default value of 'm' when power is cycled, so the enumeration command should be part of the system boot sequence.
3) The "N" serial port command optionally overrides the state of the $\overline{\text{PFC ENA}}$ input, allowing a unit to be forced on or off.
4) The Battle-Short function may be set via the serial port using the "n" command.

Control Connections for Paralleling

The following are control signal wiring recommendations for a parallel system:

1) The CTL RETURN pins from multiple units should be connected together to provide a common control ground.
2) SERIAL IN and $\overline{\text{PFC ENA}}$ input pins may be wired in parallel.
3) AC GOOD and DC GOOD output pins may be wired in parallel.
4) START SYNC should be connected in parallel between all units in the system.
5) The 3.3V AUX outputs could also be paralleled, but total current drawn from 3.3VAUX should not exceed the 100 mA rating of a single unit.
6) SYNC OUT pins should not be connected between units: doing so would cause a logic output contention.
7) The SERIAL OUT signals may be combined using an external AND gate. Alternatively, a multi-drop bus may be formed by pulling the bus low when SERIAL OUT is low, and releasing the bus when SERIAL OUT is high, returning the bus to the idle state via a pull-up resistor. The time constant of this pull-up resistor along with any parasitic capacitance must be much shorter than the baud rate.
8) $\overline{\text{BATTLE SHORT}}$ pins should not be interconnected between units. When not warning of an impending shutdown, the $\overline{\text{BATTLE SHORT}}$ pin is normally pulled low, and this could erroneously cause other units to enter the Battle-Short state. If the $\overline{\text{BATTLE SHORT}}$ protection-warning output function is used in a paralleled system, then individual signals should be combined using an OR gate. If the $\overline{\text{BATTLE SHORT}}$ protection-disable input function is used in a paralleled system, then either a separate pull-down transistor should be used for each unit, or the Battle-Short function may be accessed via the serial port. If a $\overline{\text{BATTLE SHORT}}$ pin is not used, it may be left open.

Power Connections for Paralleling

The following are power wiring recommendations for a parallel system:

1) +VOUT and –VOUT may be wired directly in parallel, but if so any common mode filtering in individual input filters will be defeated.
2) The LINE A/B/C inputs should be wired in parallel upstream of the input filters. Each PFC unit should have its own TVS bank located near the input pins.
3) +MIDBUS should *not* be connected directly in parallel between units. It is acceptable to share a single +MIDBUS holdup capacitor between multiple units by connecting multiple R||D elements (from Figure 19) in a star configuration, but doing so will defeat any common mode filtering in individual input filters. The recommended value of +MIDBUS capacitance should be placed locally at each unit.

Input Filter Design for Paralleling

The available MACF-440-3PH-UNV-MP 3-phase AC input filter module, which includes both differential-mode (DM) and common-mode (CM) stages, should only be used in those paralleled applications where the outputs of each PFC unit are individually isolated. When paralleling multiple PFC units with the outputs directly connected, multiple parallel CM filters cannot be used, because the net current through each will not balance to zero. This would cause the CM cores to saturate and ruin the CM filter performance. If the PFC outputs must be directly connected, then there must be a shared single input common-mode filter.

Power Ratings

Continuous Power Rating

Steady-state output power is rated to 5.0 kW for input line voltages above 346 Vrms (L-L). As the steady-state +MIDBUS voltage is reduced for input line voltages below 346 Vrms (L-L), the power rating is also reduced proportionately: at 150 Vrms (L-L) +MIDBUS is nominally 300 V and the corresponding power rating is 3.725 kW (see Figure 13).

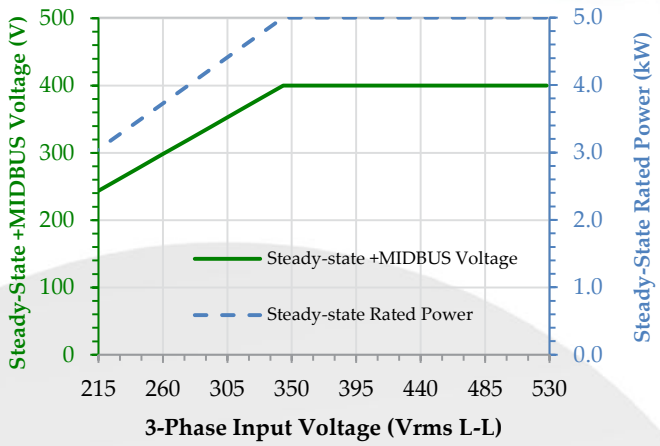


Figure 13: Steady-state +MIDBUS voltage and rated output power vs. AC line voltage. See Figure 14 for thermal derating which may further limit available power. Unit will run down to UVLO at 140 Vrms (L-L), but AC GOOD will be pulled low below 343 Vrms (L-L). AC GOOD must be valid to allow initial startup.

Thermal Management

Advanced thermal management techniques are employed to create a low thermal resistance from power devices to baseplate, while retaining SynQor's standard SMT construction and mechanically compliant potting compound. At 5 kW load and a baseplate temperature of 80 °C, the hottest internal power device runs at a junction temperature of 125 °C. This 45 °C rise is worst-case; when the baseplate is at room temperature, the same rise is only 30 °C. Using the 125 °C figure as a maximum temperature guideline yields the derating curve seen below in Figure 14.

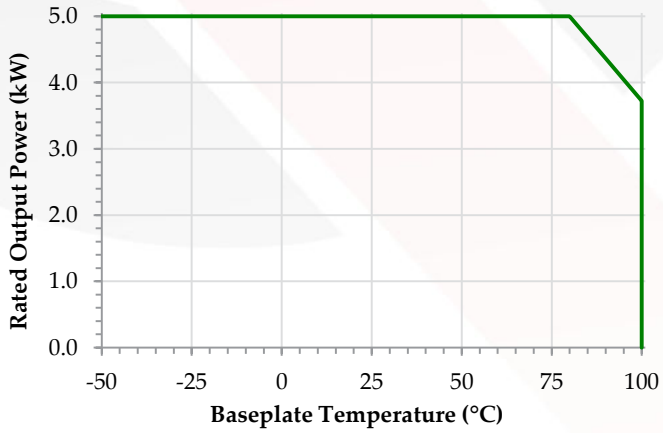


Figure 14: Rated steady state power vs. baseplate temperature. See Figure 13 for derating vs. line voltage which may further limit available power.

+MIDBUS Current Limit

The buck stage has a 22.5 A +/- 1.5 A output current limit. Thermally, operation near the current limit (above the continuous power rating shown in Figure 1) is acceptable for pulses shorter than 500 ms, but extended operation above the unit power rating can cause the unit to shut down due to over-temperature protection.

Since +VOUT is regulated, the input to the boost stage is constant-power: if +MIDBUS falls, the boost input current will rise (see Figure A for internal PFC block diagram). Therefore, if the unit is loaded from +VOUT such that the buck current limit becomes activated, the +MIDBUS voltage will collapse at a rate governed by the capacitance at +MIDBUS. It is therefore recommended to operate the converter at or below rated power in steady state, approaching current limit only during transient events.

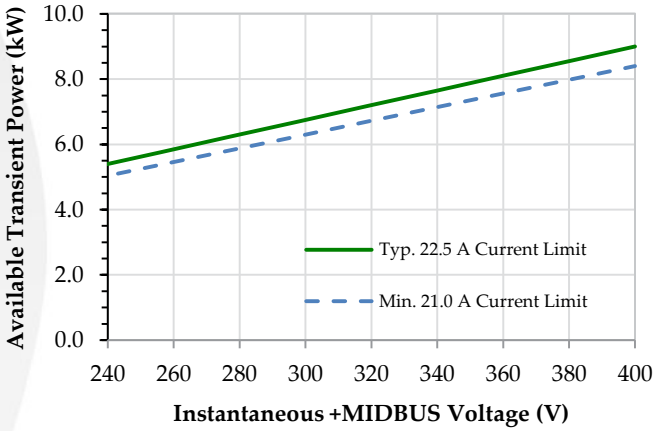


Figure 15: Available transient power vs. instantaneous +MIDBUS voltage. See Figure 13 for steady-state voltage.

Power Interrupts and Holdup

Many systems need to operate through brief interruptions of AC input power. External capacitors placed at +MIDBUS, +VOUT, or both can be used to maintain power flow to critical loads during these input power interruptions.

Holdup Capacitor Position

When the bulk holdup capacitor is located at +MIDBUS, the capacitor voltage can dip during a line dropout while +VOUT remains relatively undisturbed. The boost stage is able to maintain its normal output down to a +MIDBUS voltage of about 215 V. The voltage rating for capacitors at +MIDBUS should be at least 450 Vdc.

Holdup capacitance may instead be placed at +VOUT if dips in the output voltage are acceptable during a line interruption. During a line brownout, the diodes in the buck PFC stage

remain reverse-biased until the +MIDBUS voltage drops below the level shown in Figure 13. Using relatively low capacitance at +MIDBUS allows the +MIDBUS voltage to drop to this level quickly, allowing the converter to contribute some power to +VOUT (see Figure 15). The voltage rating for capacitors at +VOUT should be at least 450 Vdc.

The internal PFC bias supply is powered either from the AC line or from +VOUT / -VOUT. If a line interruption occurs, the unit will stay alive provided +VOUT stays above 160 V with respect to -VOUT. The boost stage includes a bypass diode so that +VOUT is never more than a diode drop below +MIDBUS.

Holdup Capacitor Value

The holdup capacitor must store a certain amount of energy:

$$E_{holdup} = P_{out} \cdot t_{drop}$$

where:

P_{out} is the output power during the holdup event

t_{drop} is the duration of the input power interruption

Based on this energy requirement, the holdup capacitor value is:

$$C_{holdup} > \frac{2 \cdot E_{holdup}}{(V_i^2 - V_f^2)}$$

where:

V_i is the initial holdup capacitor voltage immediately before the input power interruption.

V_f is the minimum capacitor voltage during the transient. (For cap at +MIDBUS, determine from Figure 15; for cap at +VOUT, determine based on downstream requirements)

The above equation is graphed in Figure 16 for holdup capacitance at +MIDBUS and Figure 17 for holdup capacitance at +VOUT.

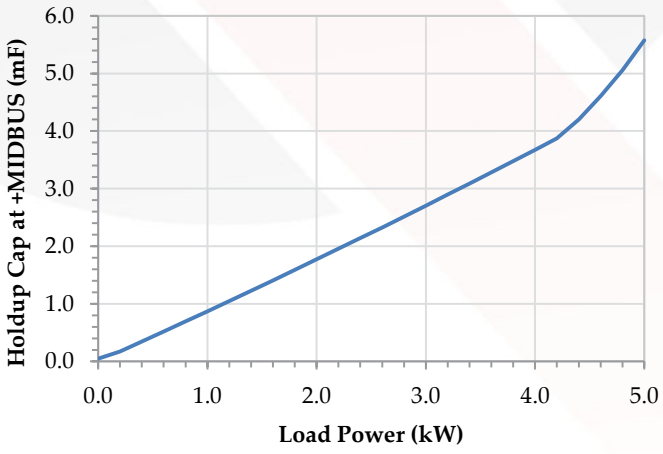


Figure 16: Minimum holdup capacitance required at +MIDBUS to ride through a 50 ms line interruption, keeping +VOUT in regulation as seen in Figure 18. Capacitor must be rated to ≥ 450 V. For capacitance above 1 mF, use R||D network as shown in Figure 19.

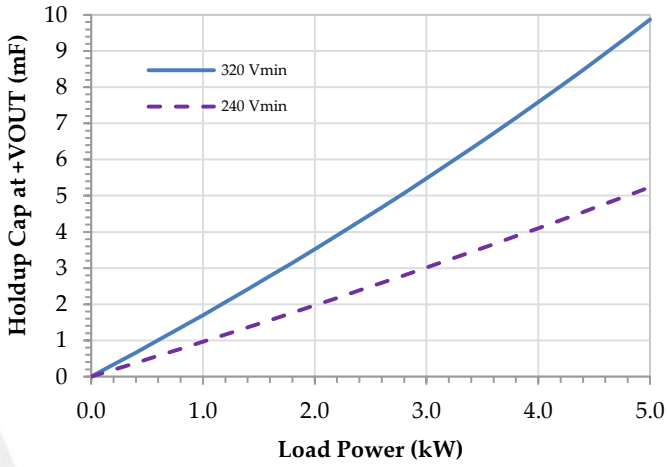


Figure 17: Minimum holdup capacitance required at +VOUT to ride through a 50 ms line interruption, allowing +VOUT to drop from 400 V nominal down to 320 V or 240 V. Capacitor must be rated to ≥ 450 V. For capacitance above 1 mF, use R||D network as shown in Figure 19.

When the holdup capacitor is located at +MIDBUS, V_i will be a function of line voltage (see Figure 13) and load current. V_f will be a function of load power during line interruption because of the +MIDBUS current limit (see Figure 15 and further discussion in the section entitled "+MIDBUS Current Limit").

Bulk holdup capacitance may also be placed at +VOUT if the system can tolerate a large voltage dip during line interruption. For instance, SynQor MCOTS-C-270H series converters have a continuous input rating down to 240 V. Almost two-thirds of the available energy can be extracted from the +VOUT capacitor as it discharges from 400 V, reducing the necessary capacitor physical volume.

SynQor MCOTS-B-270 series isolated bus converters have very high power density, but with their fixed-ratio conversion, dips at the input are reflected directly to dips at the output. It may be desired to achieve the +VOUT response shown in Figure 18 by locating bulk capacitance at +MIDBUS.

A significant safety margin on the holdup capacitor value is recommended to account for the following cumulative effects:

1) Capacitor tolerance, aging, and temperature variation
2) Capacitor ESR and diode losses during the interruption
3) Variation in the initial voltage V_i due to line & load conditions immediately preceding the input power interruption
4) Current limit tolerance (21 A minimum, which raises the required V_f to sustain load power as shown in Figure 15)
5) Fall and rise time of the input voltage, which increase the interval over which the PFC is unable to deliver power into +MIDBUS

Figure 18 shows an example of a 50 ms line interruption. Note that for the conditions in Figure 18, the ideal equation would predict C_{holdup} > 6 mF. Yet the actual capacitor used was 7.5 mF, chosen to keep the minimum voltage well above the available transient power shown in Figure 15 and to account for the combined effects of items 1, 2, 5, and 6 discussed above.

When full load is drawn during a long input power interruption, the holdup capacitor physical size quickly becomes unreasonable. Furthermore, repetitive transients require surplus energy during the recovery time. It is possible to reduce holdup power significantly by disabling non-critical loads when the AC GOOD signal goes low.

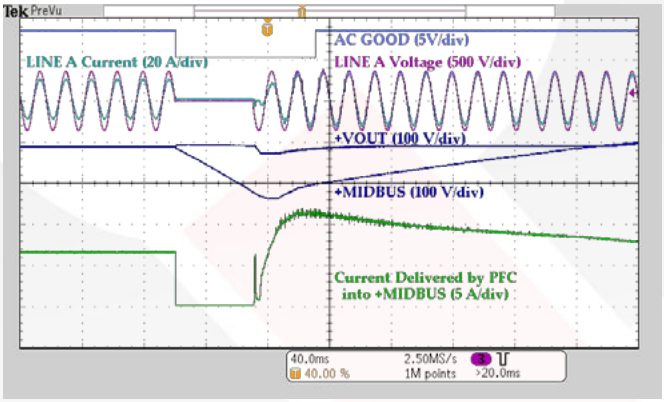


Figure 18: Response to 50 ms line interruption; 60 Hz; 5.0 kW power drawn from +VOUT pin; 7.5 mF total capacitance placed at +MIDBUS with series R || D network as shown in Figure 19.

Holdup during AC Line Brownout

When considering recovery from a line dip / brownout, t_{drop} from the above C_{holdup} equation must be carefully defined as the time during which the PFC is unable to recharge +MIDBUS. The PFC will be unable to contribute any power when +MIDBUS is above the nominal value shown in Figure 13 because diodes in the buck topology PFC stage become reversed biased and no current will flow. Therefore, during a line brownout, the +MIDBUS capacitor will need to supply the whole load demand until the +MIDBUS voltage discharges below the line shown in Figure 13 after which the buck PFC can supply up to 22.5 A (typ.) / 21.0 A (min.) into +MIDBUS.

It is possible to run through extended brownouts provided that the power demand from +MIDBUS stays below the available power shown in Figure 13. If the power exceeds this level, then the excess power must come from the +MIDBUS capacitor, and +MIDBUS voltage will collapse at a rate proportional to the excess power (and inversely proportional to the +MIDBUS capacitance). If already running, the unit will continue to run indefinitely down to 140 Vrms (L-L) (the input UVLO threshold) at reduced power, even though the AC GOOD signal is pulled low below 343 Vrms (L-L). Line voltage must be within the AC GOOD thresholds for initial startup.

Holdup during AC Line Surges

Large AC line transients can, in some cases, trip either "Short Circuit Current Limit" or "Input Over-Voltage Protection." In response, the unit will interrupt power flow for 240 µs or 1 ms, respectively. This should be treated as a line interruption; significant external holdup capacitance will typically be required to keep the output in regulation through this type of transient. See the section above entitled "Holdup Capacitor Value" for further analysis.

R||D Network for Large Holdup Capacitors

Capacitance in excess of the 1 mF maximum value requires an additional series R||D network for optimum stability, as shown in Figure 19. The diode must be rated for at least 600 V and a fast recovery type is recommended to improve forward recovery characteristics. The resistor must be adequately rated for pulse capability: a ceramic composition type is recommended.

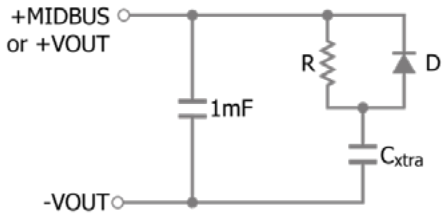


Figure 19: Series R||D network for capacitance at +MIDBUS or +VOUT in excess of 1 mF

For capacitors between 1 mF and 10 mF, the resistor value shown in Figure 19 should be 4.7 Ω. Capacitors larger than 10 mF may be used, but it is possible to trip the "+MIDBUS Under-Voltage Shutdown" protection if +MIDBUS does not reach 50 V within 150 ms after it begins to ramp up. Increasing

the resistor value to 10 Ω will circumvent this protection feature by causing the +MIDBUS voltage to quickly rise above 50 V due to the voltage drop across the resistor while in current limit. However, a 10 Ω value also increases the capacitor recharge time, affecting the ability to run through repetitive transients.

PULSED LOADS

Pulsed Loads and Input Harmonics

The CE101 input harmonics are typically measured with a DC load. If instead the system under test involved a pulsed load, the pulsed power could be reflected back to the input and might cause a compliance failure. Special constant-power control in the PFC is able to help significantly.

Conditions for Constant Input Power Control

The 3-phase PFC has two modes of control. Within +/- 20 V of the nominal +MIDBUS set point, the buck stage output approximates a constant-power characteristic. If the +MIDBUS capacitance is adequately sized, this special control forces the capacitor to absorb (and deliver) a large fraction of the load pulse energy, and thus helps prevent the load variation from appearing on the AC input lines. Within the +/- 20 V constant power window, average power flow is adjusted slowly, with a 40 ms time constant.

If on the other hand, the pulsed load is too large or +MIDBUS capacitance is too small, and +MIDBUS deviates from nominal by more than +/- 20 V, then the controller will switch modes and attempt to quickly regulate the +MIDBUS voltage. This necessarily draws transient currents from the AC input.

By way of example, consider a 1.5 kW load that pulses to 4.5 kW for 2 ms, repeating every 10 ms. This load can be considered a constant 2.1 kW superimposed with a 100 Hz repetitive transient (+2.4 kW @ 20% duty & -600 W @ 80% duty). If the +MIDBUS capacitor can supply the full transient energy (2.4 kW for 2 ms = 4.8 J) while slewing +MIDBUS by less than 40 V, the PFC input will draw essentially constant input power. Capacitor energy supplied during the transient is $\Delta E = C \cdot V \cdot \Delta V$ *or* $C = \Delta E/(V \cdot \Delta V)$. In this example, $C = 4.8\,J/(400\,V \cdot 40\,V) = 300\,uF$; when $C_{MB} > 300\,uF$, the unit will operate with constant input power.

A general solution for the minimum +MIDBUS capacitance necessary to enable constant power control may be expressed as:

$$C_{MB} > \frac{(P_{max} - P_{av}) \cdot D_{max}}{f_{tran}} \cdot \frac{1}{V_{MB} \cdot \Delta V_{MB}}$$

or

$$C_{MB} > \frac{(P_{av} - P_{min}) \cdot D_{min}}{f_{tran}} \cdot \frac{1}{V_{MB} \cdot \Delta V_{MB}}$$

where values in parenthesis are from the above example:
P_{av} is the pulsed load average power (ex. 2.1 kW)
P_{max} is the pulsed load maximum power (4.5 kW)
P_{min} is the pulsed load minimum power (1.5 kW)
D_{max} is the maximum power duty cycle (0.2)
D_{min} is the minimum power duty cycle (0.8)
f_{tran} is the pulsed load frequency (100 Hz)
V_{MB} is 400 V, the nominal +MIDBUS voltage.
ΔV_{MB} is 40 Vpk-pk, the maximum +MIDBUS voltage deviation required to maintain constant power control.

The +MIDBUS capacitor does not necessarily need to be large enough to satisfy the above equation. In applications where the load transients are small, or where AC input current transients are acceptable, less capacitance may be used at +MIDBUS, subject to the minimum value specified on page 3.

+VOUT Capacitance

Additional capacitance at +VOUT is required for applications with pulsed loads applied at +VOUT where the peak power is above 7.5 kW. In this case, the capacitance should be increased until the +VOUT capacitor sources enough of the load pulses to reduce the measured peak boost power below 7.5 kW. This prevents activation of the cycle-by-cycle boost current limit.

The minimum recommended capacitance at +VOUT varies linearly with the maximum load current. If the highest expected load current is half the rated value, then the capacitance at +VOUT may also be reduced by half. If the system draws power exclusively from +MIDBUS, then no external capacitance is required at +VOUT.

External Capacitor Selection

Capacitors connected externally at +MIDBUS and +VOUT should have a rating of 450 V or higher. Standard aluminum electrolytic capacitors are acceptable but have several significant drawbacks:

1) Increase in ESR at low temperature
2) Loss of capacitance at low temperature
3) Poor reliability at high temperature

Care must be taken to ensure that the PFC requirements for minimum output capacitance and maximum ESR are met when operating at the minimum expected temperature.

PROTECTION FEATURES

Over-Temperature Shutdown

An integrated temperature sensor protects the unit from accidental damage by disabling the unit when internal sensor temperature rises above 120 °C. The unit automatically restarts after the internal sensor cools below 115 °C. *The internal temperature may be read via the serial port at address 0x54 / 84 / "T".*

Over-temperature shutdown can be disabled (along with phase drop shutdown) by connecting the $\overline{\text{BATTLE SHORT}}$ signal to CTL RETURN. When not externally driven low, a high state on the $\overline{\text{BATTLE SHORT}}$ pin indicates that either over-temperature or phase-imbalance shutdown is imminent. The over-temperature warning threshold is 115 °C (measured at the internal sensor).

With the main over-temperature shutdown disabled, a redundant protection remains in place which will turn off both the unit and the 3.3V AUX supply when the bias supply IC temperature goes above approximately 160 °C.

Phase Imbalance Shutdown

The AC line amplitude V_{sys} is expressed internally by the controller as a function of the three instantaneous input voltages, measured from line to a pseudo-neutral:

$$V_{sys} = \sqrt{2/3} \cdot \sqrt{V_{a\,(L-N)}^2 + V_{b\,(L-N)}^2 + V_{c\,(L-N)}^2}$$

For balanced 3-phase sinusoidal line inputs, the instantaneous value of V_{sys} is constant throughout the AC line cycle:

$$V_{sys\ balanced} = \sqrt{2} \cdot V_{x\ rms\ (L-N)} = V_{x\ pk\ (L-N)} = \sqrt{2/3} \cdot V_{x\ rms\ (L-L)}$$

Any asymmetry between the three line inputs will cause V_{sys} to vary in amplitude throughout a line cycle. To calculate the largest observed amplitude variance, the maximum and minimum values of V_{sys} within each full line cycle are captured and then subtracted from each other.

$$\Delta V_{sys} = V_{sys\ max} - V_{sys\ min}$$

For balanced sinusoidal 3-phase input voltages, the instantaneous value of V_{sys} is constant, and therefore the value of ΔV_{sys} is near zero. For imbalanced or distorted input voltages, a value of ΔV_{sys} above 70 V will trigger a warning on the $\overline{\text{BATTLE SHORT}}$ pin, and if this condition persists for more than 0.25 seconds, a phase imbalance shutdown will ensue. This threshold is listed on the specification table in terms of pure amplitude imbalance or pure phase imbalance. In practice, the value of ΔV_{sys} will reflect a combination of amplitude imbalance, phase imbalance, distortion, and measurement error. For MIL-STD-1399 compliant electric power systems and indeed most AC mains, ΔV_{sys} will be quite small. However, if the expected phase imbalance or input voltage distortion is unusually poor, then the working value of ΔV_{sys} should be considered.

The digital values of ΔV_{sys} (updated every line cycle) and V_{sys} (post-filtered with a 0.25 second time-constant) may be accessed via the serial interface at addresses 0x73 / 115 / "s" and 0x53 / 83 / "S", respectively.

The complete loss of one line phase will always cause ΔV_{sys} to exceed the phase imbalance threshold. As such, the unit will attempt to deliver power from the remaining two input line phases for 0.25 seconds and then shut down (if not in battle-short mode). The unit will automatically attempt to restart approximately 1 second after normal three-phase power is restored. Phase-imbalance (and over-temperature) shutdown are disabled in battle-short mode, engaged either via the serial port or by externally connecting the $\overline{\text{BATTLE SHORT}}$ signal to CTL RETURN. In battle-short mode, the unit will attempt to deliver power throughout any imbalance or phase-drop event. While attempting to deliver power from only two phases or from a very imbalanced source, the other protection circuits (like current limit) remain active; the output voltage may ripple or sag and the input line currents may exhibit excessive distortion.

Short Circuit Current Limit

In most overload conditions, the linear 22.5 A buck current limit is sufficient. A backup "short-circuit current limit" circuit handles severe input transients or output short-circuit events. Redundant current sense resistors and comparators are connected in series with both the positive and negative sides of the buck PFC stage, set to trip well above the linear current limit threshold. When this backup protection is activated, the unit will respond by turning off all power flow from the input for approximately 240 µs, after which normal operation resumes immediately.

Input Over-Voltage Protection

If the instantaneous voltage between any two line inputs goes above the threshold of 900 V (L-L), then all power flow from the input will be interrupted, resuming 1 ms after the input voltage falls again below the same threshold. (Voltage spikes shorter than 80 µs may not trigger this protection response.) During an interruption, the +MIDBUS voltage will fall at a rate determined by capacitance and load current. The amount capacitance needed to maintain normal operation during this 1 ms interruption may be calculated as shown in the section entitled "Holdup Capacitor Value."

Boost Current Limit

An independent current sense resistor and comparator implement a hardware cycle-by-cycle current limit in the boost stage, set to a boost input current of approximately 32 A. The boost stage is in series with the buck stage, and the buck current limit is set to 22.5 A, so the boost current limit is only active in abnormal situations, such as an output short. A bypass diode is connected internally between +MIDBUS and +VOUT to provide further short-circuit protection.

Output Over-Voltage Protection

A redundant hardware over-voltage protection circuit will disable the boost stage on a cycle-by-cycle basis if +VOUT ever rises above 440 V. The unit resumes normal operation immediately after the output voltage returns below this threshold.

+MIDBUS Under-Voltage Shutdown

Should the action of the linear 22.5 A buck current limit reduce the +MIDBUS voltage to less than 50 V for more than 150 ms, the unit will assume a sustained overload and will shut down. Auto-restart will occur after 1 second. This feature is also present during startup and thus serves to limit energy delivered into a shorted output.

Pre-bias / Reverse Power Flow

Both the buck and boost stages have diode rectification that prevents reverse power flow, regardless of whether the unit is enabled or disabled. It is acceptable to start up with voltage present and/or to connect external voltage sources to +MIDBUS / +VOUT. If a downstream power converter experiences reverse power flow, the PFC module will be unable to avoid an output over-voltage condition because it cannot sink current.

EMI Recommendations

Input Filtering

It is highly recommended to pair the PFC module with the separately available MACF-440-3PH-UNV-MP high-voltage 3-phase AC input filter module, which was designed specifically to work with the PFC module. Advantages include:

- Excellent attenuation at 200 kHz
- Low differential and common mode capacitance
- Operation over full line frequency range
- PFC tuned to actively cancel filter reactive power
- Filter height and width match the PFC module

MIL-STD-461F Compliance

This module is designed specifically to meet the following sections of MIL-STD-461 revision F (given a properly designed system based on Figure A from page 2):

- CE101-2 (30 Hz – 10 kHz)
- CE102 (10 kHz – 10 MHz)
- CS101 (30 Hz – 150 kHz)
- CS106 (Pulse Transients)
- CS114 (Curve #5) (10 kHz – 200 MHz)
- CS115 (Impulse Excitation)
- CS116 (10 kHz – 100 MHz)
- RE101 (Navy Limit) (30 Hz – 100 kHz)
- RE102 (Navy Topside) (10 kHz – 1 GHz)

MIL-STD-1399 Compliance

This module is specifically designed to comply with the following items from MIL-STD-1399 section 300B (given a properly designed system based on Figure A from page 2):

- Voltage and Frequency Tolerance (¶ 5.3.1)
- Transient Tolerance and Recovery (¶ 5.3.2)
- Voltage Spikes to 2500 V (¶ 5.3.3)
- Emergency Conditions (¶ 5.3.4)
- Grounding (¶ 5.3.5)
- Power Profile (¶ 5.3.6)
- Current Waveform (¶ 5.3.7)
- Voltage and Frequency Modulation (¶ 5.3.8)
- Leakage Current (¶ 5.3.9)
- Insulation Resistance (¶ 5.3.10)

CE102 Results

Conducted emissions are presented here using the separately available MACF-440-3PH-UNV-MP high-voltage 3-phase AC input filter module, running at 60 Hz, and with 50 µH LISNs. Data are shown below for power levels of 5.0 kW, 3.0 kW, and 1.0 kW. 5 µH LISNs are recommended for testing at 400 Hz line frequency.

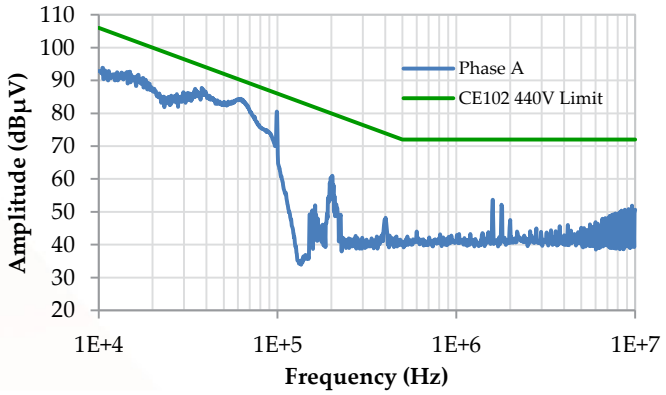


Figure 20: CE102 data at 60 Hz and 5.0 kW output power (50 µH LISNs).

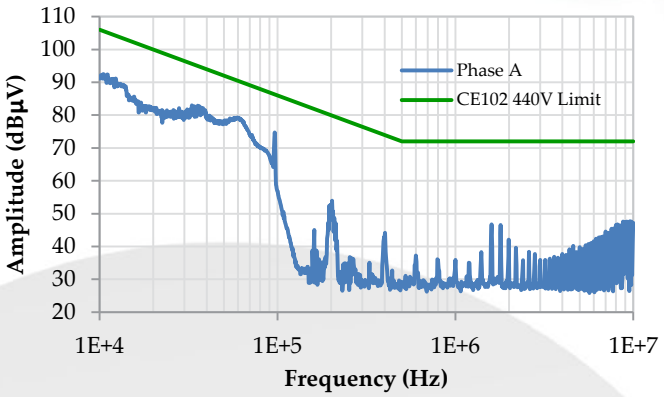


Figure 21: CE102 data at 60 Hz and 3.0 kW output power (50 µH LISNs).

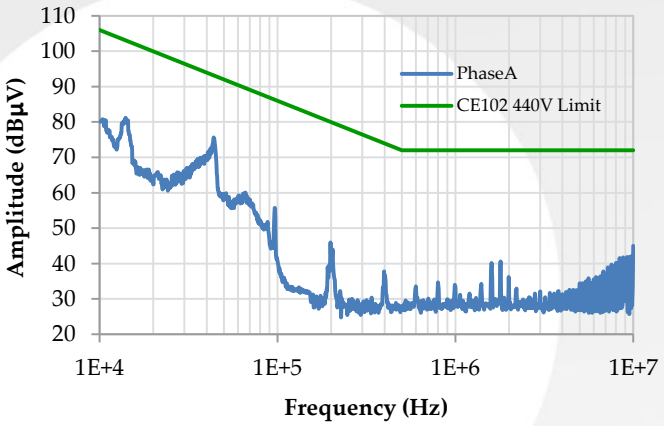


Figure 22: CE102 data at 60 Hz and 1.0 kW output power (50 µH LISNs).

Baseplate Electrical Connection

All circuitry in the PFC module is electrically isolated from the baseplate with a multi-layer solid insulator. The baseplate and corner mounting posts may therefore be connected to protective earth ground in the application circuit. Maintain adequate clearance from all external circuitry to the four corner mounting posts, which are electrically connected to the baseplate.

SHIELD (Pin 8)

The SHIELD net is internally coupled via capacitors to both the input and output voltages and is therefore able to locally contain high frequency electromagnetic emissions. If desired, this pin may be connected to a floating shield plane underneath the unit, but must always be left floating. When the unit is soldered into a PCB, this lower SHIELD plane would typically be constructed on one of the top-most PCB layers. See Figure 10 for a measurement of the typical voltage seen on the SHIELD net.

Control Pins

START SYNC (Pin A1)

Pin A1, designated as START SYNC, should be connected as a bus between all paralleled units to synchronize restart after a fault condition. This pin should be left floating when not used. See section entitled "Control Features" for further details. Internal interface circuitry is shown in Figure 26.

CTL RETURN (Pin A2)

CTL RETURN serves as the ground reference for all user control signals. Basic insulation is provided between the ten user control pins and the ten power pins. CTL RETURN may be externally connected to any of the power pins, attached to an application circuit, or left floating. An additional stage of external isolation will be needed if interfacing to a touchable net. Any external safety-rated isolators could be powered from 3.3V AUX, simplifying implementation.

SERIAL IN (Pin A3)

A wide variety of operating parameters (voltages, currents, temperatures) may be accessed via the built-in full-duplex asynchronous serial interface. It is also possible control to the $\overline{\text{BATTLE SHORT}}$ and $\overline{\text{PFC ENA}}$ pin functions via the serial interface. Commands may be transferred to the internal DSP via the SERIAL IN pin at 9600 baud (8N1 – 8 data bits, no parity, 1 stop bit). A `start' or `zero' bit is encoded as a logic low. The internal baud rate will be exactly 20.48 times lower than the SYNC OUT frequency. The tolerance of both frequencies is better than +/- 2%. The frequency tolerance of the external interface circuit should also be better than +/- 2% accuracy to ensure that the last bit of incoming serial data arrives within the proper frame time. Alternatively, the SYNC OUT signal may be used to continuously calibrate the baud rate of the external interface circuit, allowing the use of a less accurate oscillator.

The SERIAL IN pin may be left open if unused, and will be internally pulled up to 3.3V AUX, corresponding to the `idle' or `stop' state. Internal circuitry is shown in Figure 23. Direct connection may be made to an external microcontroller, but an external transceiver IC is required to shift levels and polarity to drive from a standard RS-232 port. Safety isolation may be achieved using just one external digital isolator channel since there is no clock signal and the input/output direction is well defined. See the separate "MPFC-440-3PH-400-LE Serial Interface" companion document for detailed command syntax (available at www.synqor.com/MPFC-440-3PH-400-LE_Serial_Interface).

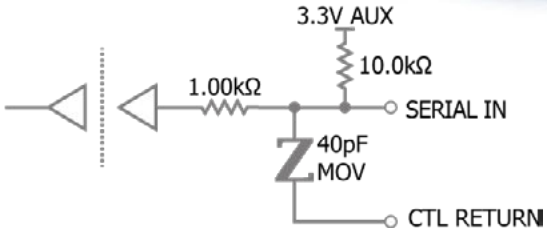


Figure 23: Internal circuitry for SERIAL IN pin.

SERIAL OUT (Pin A4)

A response to each command is sent via the SERIAL OUT pin at 9600 baud (8N1 – 8 data bits, no parity, 1 stop bit). The output is low for a `start' or `zero' bit. When not transmitting, the output is high, corresponding to the `idle' or `stop' state. Internal circuitry is shown in Figure 27. Direct connection may be made to an external microcontroller, but an external transceiver IC is required to shift levels and polarity to drive a standard RS-232 port. See the separate "MPFC-440-3PH-400-LE Serial Interface" companion document for detailed response syntax (available at www.synqor.com/MPFC-440-3PH-400-LE_Serial_Interface).

AC GOOD (Pin A5)

The unit will not turn on until the positive-logic AC GOOD output is high. Input voltage levels, frequency, and distortion must all be within the specified limits.

AC GOOD generally only serves as a power interruption warning: the unit will continue to run even if AC GOOD transitions low. The response time of AC GOOD to an input power interruption is less than 1 ms at 400 Hz and less than 5 ms at 60 Hz. AC GOOD will return to its normal high state about 40 ms after the line voltage recovers. See Figure 18 for an example of AC GOOD timing during a power interruption. Internal interface circuitry is shown in Figure 24.

DC GOOD (Pin A6)

During startup the positive-logic DC GOOD output will remain low until +VOUT crosses the specified rising threshold (see Figure 9). The falling threshold is significantly lower, such that DC GOOD will usually remain high during an input power interruption. Therefore, DC GOOD is typically used to indicate successful startup, whereas AC GOOD is used to warn of an input power interruption. The typical DC GOOD response time is less than 1 ms. Internal interface circuitry is shown in Figure 24.

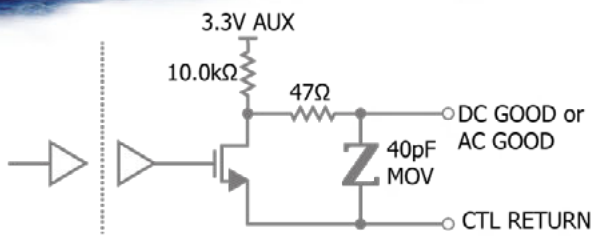


Figure 24: Internal circuitry for AC GOOD and DC GOOD pins.

$\overline{\text{PFC ENA}}$ (Pin A7)

The $\overline{\text{PFC ENA}}$ pin must be brought low to enable the unit. A 10.0 kΩ pull-up resistor is connected internally to 3.3V AUX. Therefore, if all control pins are left floating, the unit will be disabled. The delay from enable to the beginning of the startup ramp is typically 300 ms (see Figure 9). Internal interface circuitry is shown in Figure 25.

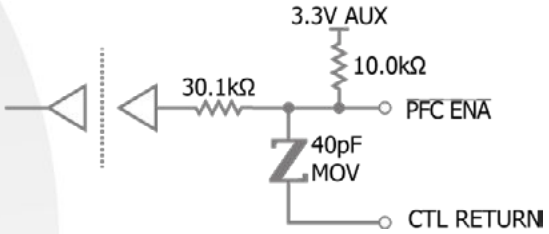


Figure 25: Internal circuitry for $\overline{\text{PFC ENA}}$ pin.

$\overline{\text{BATTLE SHORT}}$ (Pin A8)

If the $\overline{\text{BATTLE SHORT}}$ pin is externally pulled down to CTL RETURN, over-temperature protection and phase drop shutdown will be disabled. If the $\overline{\text{BATTLE SHORT}}$ pin is not externally held low, the pin will go high to warn of either an impending over-temperature shutdown or an input phase drop shutdown. The battle-short function may be engaged via the serial port (instead of shorting the pin) to maintain use of the warning output. The over-temperature warning engages 5 °C below shutdown. The input phase drop warning engages 250 ms before shutdown. A 10.0 kΩ pull-up resistor is connected internally to 3.3V AUX. Internal interface circuitry is shown in Figure 26.

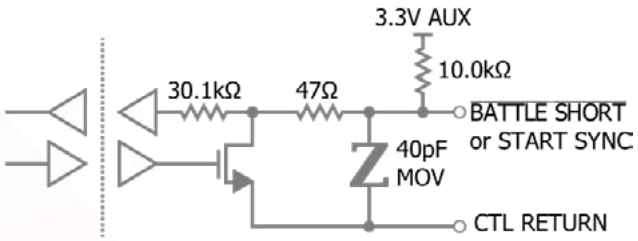


Figure 26: Internal circuitry for $\overline{\text{BATTLE SHORT}}$ and START SYNC pins.

3.3V AUX (Pin A9)

The 3.3V AUX supply is energized whenever AC power is present, regardless of the $\overline{\text{PFC ENA}}$ state, and is rated up to 100 mA at 3.3 V (relative to CTL RETURN). This independent supply is powered from either the line input or main output. Therefore, if there is a line interruption but the +VOUT output voltage remains above 160 Vdc due to external holdup capacitance (at +VOUT or +MIDBUS), the 3.3V AUX output will remain live. With the output disabled and with only 2 of 3 valid input line phases, there is adequate internal energy storage to keep the 3.3V AUX output in normal regulation if the line frequency is 400 Hz. With only 1 of 3 valid input line phases, the bias supply will typically shut down and periodically attempt to restart.

Some internal circuitry is also powered by 3.3V AUX, so if 3.3V AUX is externally shorted, the unit will be disabled.

SYNC OUT (Pin A10)

The SYNC OUT pin generates a continuous series of pulses at the main switching frequency. The duty cycle may (intentionally) vary between 5% and 50%, so only the rising edge should be used as a timing reference. The buck and boost converters are synchronized and switch at the same frequency. The SYNC OUT pin may be left open if not used. Internal interface circuitry is shown in Figure 27.

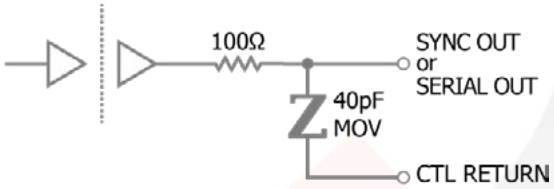
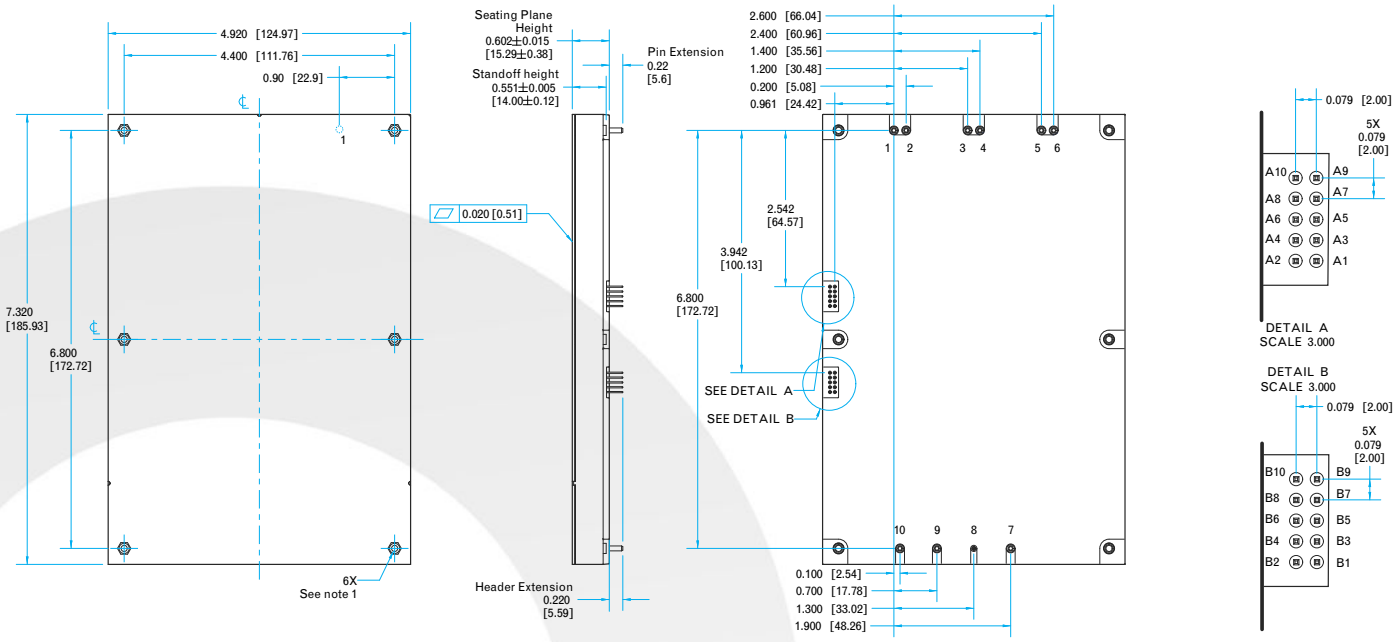


Figure 27: Internal circuitry is identical for SYNC OUT and SERIAL OUT pins.

MPFC-440-3PH-400-LE

Input:3Φ 360-528 Vrms (L-L)
Output:400 Vdc
Power:5.0 kW



NOTES:

1. APPLIED TORQUE PER M3 SCREW SHOULD NOT EXCEED 6 in-lb (0.7 Nm)
2. BASEPLATE FLATNESS TOLERANCE IS 0.020" (.51mm) TIR FOR SURFACE
3. PINS 1-7, 9, AND 10 ARE 0.080" (2.03 mm) DIA. WITH 0.125" (3.18 mm) DIA. STANDOFF SHOULDERS
   MATERIAL: COPPER ALLOY. FINISH: MATTE TIN OVER NICKEL PLATING
4. PIN 8 IS 0.040" (1.02 mm) DIA. WITH 0.080" (2.03MM) DIA. STANDOFF SHOULDERS
   MATERIAL: COPPER ALLOY. FINISH: MATTE TIN OVER NICKEL PLATING
5. PINS A1-A10 AND B1-B10 ARE 0.020" X 0.020" (0.51mm X 0.51mm)
   MATERIAL: PHOSPHOR BRONZE. FINISH: GOLD FLASH OVER NICKEL UNDERPLATING
6. UNDIMENSIONED COMPONENTS ARE SHOWN FOR VISUAL REFERENCE ONLY.
7. ALL DIMENSIONS IN INCHES (mm)
   TOLERANCES: X.XX IN +/-0.020 (X.X mm +/-0.5 mm)
   X.XXX IN +/-0.010 (X.XX mm +/-0.25 mm)
8. WEIGHT: 36 oz (1020 g)

PIN DESIGNATIONS

Pin	Label	Name	Function
1	TVS A	TVS A	AC Line A Tap at Power Switch (for External TVS)
2	LINE A	LINE A	AC Line A Power Input
3	TVS B	TVS B	AC Line B Tap at Power Switch (for External TVS)
4	LINE B	LINE B	AC Line B Power Input
5	TVS C	TVS C	AC Line C Tap at Power Switch (for External TVS)
6	LINE C	LINE C	AC Line C Power Input
7	-VOUT	-VOUT	Negative Return for +VOUT and +MIDBUS
8	SHIELD	SHIELD	EMI Shield - Leave Floating
9	+MIDBUS	+MIDBUS	Positive PFC Output / Boost Input Voltage
10	+VOUT	+VOUT	Positive Boost Output Voltage
A1	START SYNC	START SYNC	Startup Synchronization / Address Enumeration
A2	CTL RETURN	CTL RETURN	Isolated Ground Reference for Pins A1 - A10
A3	SERIAL IN	SERIAL IN	Serial Data Input (High = Stop/Idle)
A4	SERIAL OUT	SERIAL OUT	Serial Data Output (High = Stop/Idle)
A5	AC GOOD	AC GOOD	AC Power Good Output (High = Good)
A6	DC GOOD	DC GOOD	DC Power Good Output (High = Good)
A7	$\overline{\text{PFC ENA}}$	PFC ENA	Pull Low to Enable Unit
A8	$\overline{\text{BATTLE SHORT}}$	BATTLE SHORT	Pull Low to Disable OTP / Phase Drop Shutdown
A9	3.3V AUX	3.3V AUX	3.3V @ 100mA Always-On Power Output
A10	SYNC OUT	SYNC OUT	Switching Frequency Synchronization Output
B1 - B10	RESERVED	RESERVED	Do Not Connect (Referenced to LINE A/B/C) - Maintain Adequate Creepage & Clearance

Part Numbering Scheme						
Family	**Input Voltage**	**Output**	**Package Size**	**Thermal Design**	**Screening Level**	**Options**
MPFC	**440-3PH:** 3-Phase 440 Vrms L-L	**400:** 400 Vdc	**LE:** Large-Module Exa	**D**: Non-Threaded	**S:** S-Grade **M:** M-Grade	**[ ]:** Standard Feature

Example: MPFC-440-3PH-400-LE-D-M

PART NUMBERING SYSTEM

The part numbering system for SynQor's ac-dc converters follows the format shown in the example.

APPLICATION NOTES

A variety of application notes and technical white papers can be downloaded in PDF format from our website.

PATENTS

SynQor holds numerous U.S. patents, one or more of which apply to most of its power conversion products. Any that apply to the product(s) listed in this document are identified by markings on the product(s) or on internal components of the product(s) in accordance with U.S. patent laws. SynQor's patents include the following:

6,896,526 6,927,987 7,050,309 7,765,687

7,787,261 8,149,597 8,644,027

WARRANTY

SynQor offers a two (2) year limited warranty. Complete warranty information is listed on our website or is available upon request from SynQor.